What is claimed is:

1. Control method of a non-volatile semiconductor memory cell an operation cycle of which consists of a bias-application period for applying bias voltage for data-erase or data-write and a verification period for making a result verification after termination of the bias-application period, and pluralities of the operation cycles of which are repeated for erase operation and write operation to the non-volatile semiconductor memory cell, the control method comprising steps of:

bias adjustment step where the bias voltage becomes deeper by increment of operation unit including at least one operation cycle along with progress of the erase operation or the write operation and duration of the operation unit is controlled to have positive correlation to voltage difference of preceding operation unit and the bias voltage; and

verification step where the operation cycle becomes shortest at a stage near end of the erase operation or the write operation.

2. Control method of a non-volatile semiconductor memory cell according to claim 1, wherein, in the bias adjustment step, duration of the operation unit is adjusted depending on time that current for data-erase or data-write carried out by applying bias voltage to the non-volatile semiconductor memory cell decreases to a predetermined current value.

3. Control method of a non-volatile semiconductor memory cell according to claim 1, wherein, in the operation unit that is to reach the verification step, the operation cycle becomes shorter by increment of operation unit.

4. Control method of a non-volatile semiconductor memory cell according to claim 1, wherein, in the bias adjustment step, voltage difference of the bias voltage between the operation units adjacent to each other and duration of the operation unit are same between the operation units adjacent to each other.

5. Control method of a non-volatile semiconductor memory cell according to claim 1, wherein, in the bias adjustment step, voltage difference of the bias voltage between the operation units adjacent to each other and total time of the bias-application period of the operation unit are same between the operation units adjacent to each other.

6. Control method of a non-volatile semiconductor memory cell an operation cycle of which consists of a bias-application period for applying bias voltage for data-erase or data-write and verification period for making a result verification after termination of the bias-application period, and pluralities of the operation cycles of which are repeated for erase operation and write operation to the non-volatile semiconductor memory cell, the control method comprising steps of:

first bias adjustment step where, during a first predetermined period that begins with start of either the erase operation or the write operation, the bias voltage becomes deeper by increment of operation unit including at least one operation cycle along with progress of the erase operation or the write operation and duration of the operation unit is controlled to have positive correlation to voltage difference of preceding operation unit and the bias voltage; and

second bias adjustment step where, during a second predetermined period that comes near with end of either the erase operation or the write operation, the bias voltage becomes deeper by increment of operation unit including at least one operation cycle along with progress of the erase operation or the write operation and duration of operation unit is controlled to be short compared with adjustment time taken by the first bias adjustment step.

7. Control method of a non-volatile semiconductor memory cell an operation cycle of which consists of a bias-application period for applying bias voltage for data-erase or data-write and verification period for making a result verification after termination of the bias-application period, and pluralities of the operation cycles of which are repeated for erase operation and write operation to the non-volatile semiconductor memory cell, the control method comprising steps of:

first bias adjustment step where, during a first predetermined period that begins with start of either the erase operation or the write operation, the bias voltage becomes deeper by increment of operation unit including at least one operation cycle along with progress of the erase operation or the write operation and duration of the operation unit is controlled to have positive correlation to voltage difference of preceding operation unit and the bias voltage; and

third bias adjustment step where, during a third predetermined period that comes near with end of either the erase operation or the write operation, voltage difference of the bias voltage between operation units including at least one the operation cycles becomes deeper than voltage difference of

the bias voltage in the first bias adjustment step.

8. Control method of a non-volatile semiconductor memory cell according to claim 6, wherein a period of the operation cycle is constant in the first bias adjustment step and the second bias adjustment step.

9. Control method of a non-volatile semiconductor memory cell according to claim 6 or 7 further comprising verification step where a period of the operation cycle becomes shortest at a stage near end of the erase operation or the write operation.

10. Control method of a non-volatile semiconductor memory cell according to claim 6, wherein,

in the first bias adjustment step, duration of the operation unit is adjusted depending on time that current for data-erase or data-write carried out by applying the bias voltage to the non-volatile semiconductor memory cell decreases to a predetermined current value, and

in the second bias adjustment step, duration of the operation unit is adjusted before time that current for data-erase or data-write carried out by applying the bias voltage to the non-volatile semiconductor memory cell reaches the predetermined current value.

11. Control method of a non-volatile semiconductor memory cell according to claim 9, wherein the verification step is conducted in the second bias adjustment step.

12. Control method of a non-volatile semiconductor memory cell

according to claim 6, wherein, in the second bias adjustment step, duration of the operation unit is shortened compared with duration of a previous operation unit.

13. Control method of a non-volatile semiconductor memory cell according to claim 12, wherein, in the second bias adjustment step, number of the operation cycles in the operation unit decreases compared with number of the operation cycles in the previous operation unit.

14. Control method of a non-volatile semiconductor memory cell according to claim 12, wherein, the previous operation unit is an operation unit preceding to the operation unit.

15. Control method of a non-volatile semiconductor memory cell according to claim 6, wherein, in the second bias adjustment step, voltage difference of the bias voltage between succeeding operation units is equal.

16. Control method of a non-volatile semiconductor memory cell according to claim 6, wherein, in the second bias adjustment step, voltage difference of the bias voltage between the succeeding operation units increases compared with voltage difference of the bias voltage previous succeeding operation units.

17. Control method of a non-volatile semiconductor memory cell according to claim 16, wherein the previous operation unit is an operation unit preceding to the operation unit.

18. A non-volatile semiconductor memory device for conducting erase operation or write operation to a non-volatile semiconductor memory cell by repeating an operation cycle of which consists of a bias-application period to apply bias voltage for data-erase or data-write and a verification period to make a result verification after termination of the bias-application period, the non-volatile semiconductor memory device comprising:

a control parameter setting section for setting a control parameter for the erase operation or the write operation; and

a control section for controlling the erase operation or the write operation in accordance with the control parameter from the control parameter setting section.

19. A non-volatile semiconductor memory device according to claim 18, wherein the control parameter setting section includes a memory section in which the control parameter can be set from outside of the device.

20. A non-volatile semiconductor memory device according to claim 19, wherein the memory section is rewritable.

21. A non-volatile semiconductor memory device according to claim 18, wherein the control parameter holds true with at least one of followings:

(a) the bias voltage applied to the non-volatile semiconductor memory cell for the erase operation or the write operation; or

(b) duration of the bias-application period; or

(c) times of the operation cycles; or

(d) initial bias voltage in case the bias voltage is changed; or

(e) final bias voltage in case the bias voltage is changed; or

(f) voltage difference between bias voltages.

22. A non-volatile semiconductor memory device according to claim 18, wherein, in an erase characteristic operation or a write characteristic operation, the control parameter is set based on time to verify termination of an erase operation or termination of write operation and bias condition until the termination.